WHAT IS CLAIMED IS:

1. A method of fabricating a SiGe thin layer semiconductor structure, the method comprising:

providing a substrate having a dielectric layer thereon to a process chamber of a processing system;

forming a variable composition Si_xGe_{1-x} layer over the dielectric layer; and

forming a Si cap layer on the variable composition Si_xGe_{1-x} layer.

2. The method according to claim 1, wherein the substrate comprises one of a semiconductor substrate, a LCD substrate, and a glass substrate.

3. The method according to claim 1, wherein the dielectric layer comprises at least one of an oxide layer, a nitride layer, an oxynitride layer, and a high-k layer.

4. The method according to claim 1, wherein the variable composition Si_xGe_{1-x} layer comprises at least one of a graded Si_xGe_{1-x} layer with a graded Ge content and a plurality of Si_xGe_{1-x} sub-layers each with different Ge content.

5. The method according to claim 4, wherein the graded Ge content in the Si_xGe_{1-x} layer is less than about 0.5.

6. The method according to claim 4, wherein the different Ge contents in the Si_xGe_{1-x} sublayers are less than about 0.5.

7. The method according to claim 4, wherein the different Ge contents in the Si_xGe_{1-x} sub-layers are less than about 0.3.

8. The method according to claim 1, wherein forming the variable composition Si_xGe_{1-x} layer includes providing a graded Ge content, with the Ge content being in the range of about 0.2 to about 0.5 adjacent the dielectric layer and decreasing to a value of 0.1 or less adjacent the Si cap layer.

9. The method according to claim 1, wherein the variable composition Si_xGe_{1-x} layer comprises a first Si_xGe_{1-x} sublayer formed on the dielectric layer, the first Si_xGe_{1-x} sublayer having a Ge content between about 0.5 and about 0.3, and a second Si_xGe_{1-x} sublayer formed on the first Si_xGe_{1-x} sublayer, the second Si_xGe_{1-x} sublayer having a Ge content between about 0.15 and about 0.05.

10. The method according to claim 1, wherein the variable composition Si_xGe_{1-x} layer comprises a first Si_xGe_{1-x} sublayer formed on the dielectric layer, the first Si_xGe_{1-x} sublayer having a Ge content of about 0.2, and a second Si_xGe_{1-x} sublayer formed on the first Si_xGe_{1-x} sublayer, the second Si_xGe_{1-x} sublayer having a Ge content of about 0.1.

11. The method according to claim 1, wherein the providing comprises introducing a substrate into one of a process chamber of a single wafer processing system and a process chamber of a batch-type processing system.

12. The method according to claim 1, wherein the forming a variable composition Si_xGe_{1-x} layer comprises exposing the substrate to a Si-containing gas and a Ge-containing gas in a chemical vapor deposition process.

13. The method according to claim 11, wherein the Si-containing gas comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, and Si_2Cl_6, and the Ge-containing gas comprises at least one of GeH_4 and $GeCl_4$.

14. The method according to claim 1, wherein the forming a Si cap layer comprises exposing the substrate to at least one of SiH_4, Si_2H_6, SiH_2Cl_2, and Si_2Cl_6 in a chemical vapor deposition process.

15. The method according to claim 1, further comprising:

forming a Si-containing seed layer on the dielectric layer, wherein the variable composition Si_xGe_{1-x} layer is formed on the Si-containing seed layer.

16. The method according to claim 15, wherein the Si-containing seed layer comprises one of amorphous Si and poly-Si.

17. The method according to claim 15, wherein the Si-containing seed layer comprises a Si_xGe_{1-x} layer.

18. The method according to claim 15, wherein the Si-containing seed layer comprises a Si_xGe_{1-x} layer with Ge content of about 0.1, or less.

19. The method according to claim 15, wherein the forming a Si-containing seed layer comprises exposing the substrate to a Si-containing gas containing at least one of SiH_4, Si_2H_6, SiH_2Cl_2, and Si_2Cl_6 in a chemical vapor deposition process.

20. The method according to claim 19, wherein the exposing further comprises exposing the substrate to an inert gas.

21. The method according to claim 19, wherein the exposing further comprises exposing the substrate to H_2.

22. The method according to claim 15, wherein the forming a Si-containing seed layer comprises performing an atomic layer deposition process.

23. The method according to claim 22, wherein the forming a Si-containing seed layer comprises alternately exposing the substrate to a Si-containing gas and H_2.

24. The method according to claim 22, wherein the forming a Si-containing seed layer comprises alternately exposing the substrate to a Si-containing gas, H_2, and a Ge-containing gas.

25. The method according to claim 1, wherein the forming further comprises heating the substrate to between about 500°C and about 900°C.

26. The method according to claim 1, further comprising providing a process chamber pressure less than about 100Torr.

27. The method according to claim 1, further comprising providing a process chamber pressure less than about 1Torr.

28. A computer readable medium containing program instructions for execution on a processor, which when executed by the processor, cause a processing apparatus to perform the steps in the method recited in claim 1.

29. A computer readable medium containing program instructions for execution on a processor, which when executed by the processor, cause a processing apparatus to perform the steps in the method recited in claim 15.

30. A SiGe thin layer semiconductor structure comprising:
a substrate having a dielectric layer thereon;
a variable composition Si_xGe_{1-x} layer over the dielectric layer; and
a Si cap layer on the variable composition Si_xGe_{1-x} layer.

31. The thin layer semiconductor structure according to claim 30, wherein the substrate comprises one of a semiconductor substrate, a LCD substrate, and a glass substrate.

32. The thin layer semiconductor structure according to claim 30, wherein the dielectric layer comprises at least one of an oxide layer, a nitride layer, an oxynitride layer, and a high-k layer.

33. The thin layer semiconductor structure according to claim 30, wherein the variable composition Si_xGe_{1-x} layer comprises at least one of a graded Si_xGe_{1-x} layer with a graded Ge content and a plurality of Si_xGe_{1-x} sub-layers each with different Ge content.

34. The thin layer semiconductor structure according to claim 33, wherein the graded Ge content in the Si_xGe_{1-x} layer is less than about 0.5.

35. The thin layer semiconductor structure according to claim 33, wherein the thickness of the graded Si_xGe_{1-x} layer is between about 600Å and about 1000Å.

36. The thin layer semiconductor structure according to claim 33, wherein the different Ge contents in the Si_xGe_{1-x} sublayers are less than about 0.5.

37. The thin layer semiconductor structure according to claim 33, wherein the different Ge contents in the Si_xGe_{1-x} sub-layers are less than about 0.3.

38. The thin layer semiconductor structure according to claim 30, wherein the thickness of each Si_xGe_{1-x} sublayer is between about 300Å and about 500Å.

39. The thin layer semiconductor structure according to claim 30, wherein the variable composition Si_xGe_x layer includes a graded Ge content, with the Ge content being in the range of about 0.2 to about 0.5 adjacent the dielectric layer and decreasing to a value of 0.1 or less adjacent the Si cap layer.

40. The thin layer semiconductor structure according to claim 30, wherein the variable composition Si_xGe_{1-x} layer comprises a first Si_xGe_{1-x} sublayer formed on the dielectric layer, the first Si_xGe_{1-x} sublayer having a Ge content between about 0.5 and about 0.3, and a second Si_xGe_{1-x} sublayer formed on the first Si_xGe_{1-x} sublayer, the second Si_xGe_{1-x} sublayer having a Ge content between about 0.15 and about 0.05.

41. The thin layer semiconductor structure according to claim 30, wherein the variable composition Si_xGe_{1-x} layer comprises a first Si_xGe_{1-x} sublayer formed on the dielectric layer, the first Si_xGe_{1-x} sublayer having a Ge content of about 0.2, and a second Si_xGe_{1-x} sublayer formed on the first Si_xGe_{1-x} sublayer, the second Si_xGe_{1-x} sublayer having a Ge content of about 0.1.

42. The thin layer semiconductor structure according to claim 30, wherein the variable composition Si_xGe_{1-x} layer is formed by exposing the substrate to a Si-containing gas and a Ge-containing gas in a chemical vapor deposition process.

43. The thin layer semiconductor structure according to claim 42, wherein the Si-containing gas comprises at least one of SiH_4, Si_2H_6, SiH_2Cl_2, and Si_2Cl_6, and the Ge-containing gas comprises at least one of GeH_4 and $GeCl_4$.

44. The thin layer semiconductor structure according to claim 30, further comprising:

a Si-containing seed layer between the dielectric layer and the variable composition Si_xGe_{1-x} layer.

45. The thin layer semiconductor structure according to claim 44, wherein the Si-containing seed layer comprises one of amorphous Si and poly-Si.

46. The thin layer semiconductor structure according to claim 44, wherein the Si-containing seed layer comprises a Si_xGe_{1-x} layer with Ge content of about 0.10, or less.

47. The thin layer semiconductor structure according to claim 44, wherein the thickness of the Si-containing seed layer is between about 25Å and about 50Å.

48. A processing tool for fabricating a SiGe thin layer semiconductor structure comprising:

at least one processing system configured to form a variable composition Si_xGe_{1-x} layer on a substrate having a dielectric layer thereon and to form a Si cap layer on the variable composition Si_xGe_{1-x} layer;

a transfer system configured for transferring the substrate; and

a controller configured to control the processing tool.

49. The processing tool according to claim 48, wherein the at least one processing system is further configured to form a Si-containing seed layer on the dielectric layer.

50. The processing tool according to claim 48, wherein the processing system comprises one of a batch-type processing system and a single wafer processing system.

51. The processing tool according to claim 48, further comprising a process monitoring system.

52. A processing tool for fabricating a SiGe thin layer semiconductor structure, comprising:

means for providing a substrate having a dielectric layer thereon to a process chamber of a processing system;

means for forming a variable composition Si_xGe_{1-x} layer over the dielectric layer; and

means for forming a Si cap layer on the variable composition Si_xGe_{1-x} layer.

53. The processing tool according to claim 52, further comprising:
means for forming a Si-containing seed layer on the dielectric layer.